IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Patent Application

Applicant(s): Jose A. Tierno
Docket No.: YOR920030375US1
Serial No.: 10/668,562
Filing Date: September 23, 2003
Group: 2611
Examiner: Leila Malek

Title: Methods and Apparatus For Snapshot-Based Equalization of a Communications Channel

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REMARKS FOR PRE-APPEAL BRIEF REQUEST FOR REVIEW

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

Applicants request review of the final rejection, dated September 19, 2007, in the above-identified application. No amendments are being filed with this request. A Notice of Appeal is submitted concurrently herewith.

In the present final Office Action, the Examiner has maintained the rejections raised in the non-final Office Action dated April 3, 2007. In this response, Applicants again respectfully traverse the various rejections for at least the following reasons.

Applicants submit that the Examiner has failed to establish a proper case of obviousness in the §103(a) rejection of claims 1, 3, 9-11, 13 and 19-23 over Ariyavisitakul and Thon, in that the Ariyavisitakul and Thon references, even if assumed to be combinable, fail to teach or suggest all the claim limitations, and in that no cogent motivation has been identified for combining the references or modifying the reference teachings to reach the claimed invention.

Independent claim 1 is directed to a method of equalizing an input signal received from a communications channel, comprising the steps of: generating at least one sampling from the received input signal based on a clock signal unrelated to a clock signal used to recover data associated with the received input signal; and compensating for distortion associated with the communications channel based on at least a portion of the at least one generated sampling.

In an illustrative embodiment of the present invention (FIG. 4), equalization system 400 receives an input signal from the data communications channel. The input signal is provided to programmable filter 402 whose filtering characteristics are set by filter parameters. The values for the filter parameters are provided by equalization algorithm 406. The filtering characteristics of filter 402 are adaptively set such that distortion associated with the communications channel is compensated for, i.e., canceled or, at least, substantially canceled. That is, the input signal is modified by programmable filter 402, based on the filter parameters calculated by equalization algorithm 406, to compensate for channel distortion. Snapshot module 404 samples the output of programmable filter 402, based on a clock (low-frequency sampling clock) that is unrelated to (e.g., independent of) the clock used to recover data, and provides a snapshot of the input signal to equalization algorithm 406 such that the algorithm can adapt the filter parameters, based on the snapshot, so as to compensate for distortion in the input signal caused by the channel. The adaptive loop of sampling the input signal (via snapshot module 404), adjusting the filter parameter values (via equalization algorithm 406) and applying the filtering parameter values (via programmable filter 402) to modify the input signal may continue until distortion in the input signal equals or falls below some maximum acceptable distortion threshold value. Thus, given the particular equalization algorithm and the compensation mechanism (e.g., programmable filter) used, one of ordinary skill in the art will readily realize how the particular equalization algorithm generates the compensation parameters used to equalize the input signal, based on the set of samples (snapshot) generated according to the invention.

Thus, as further explained at page 9, lines 12-20, of the present specification, by using a sampling clock that is independent of (unrelated to) the clock and data recovery (CDR) circuit of the receiver, the claimed equalization technique can operate stand-alone, i.e., without needing

input from the CDR circuit for operation.

The Examiner, in formulating the §103(a) rejection of claim 1, argues that each and every one of the above-noted limitations of claim 1 is met by the collective teachings of Ariyavisitakul and Thon. Below, Applicants explain how such portions of Ariyavisitakul and Thon fail to teach or suggest what the Examiner contends that they teach or suggest. While Applicants may refer from time to time to each reference alone in describing its deficiencies, it is to be understood that such arguments are intended to point out the overall deficiency of the cited combination.

The relied-upon portions of Ariyavisitakul do not meet certain limitations of claim 1, as alleged, for at least the reasons set forth by Applicants in their previous response dated January 31, 2007. The Examiner looks to the Thon reference to supplement the above-noted deficiencies of Ariyavisitakul as applied to claim 1. However, the Thon reference also fails to teach or suggest "generating at least one sampling from the received input signal based on a clock signal unrelated to a clock signal used to recover data associated with the received input signal," as recited in claim 1. The Examiner refers to column 3, lines 8-13 of Thon as disclosing a clock signal unrelated to a clock signal used to recover data associated with the received input signal. Column 3, lines 2-16 states the following:

> As shown in FIG. 1, a signal, such as a serial data stream, is input to a FIR equalizer circuit 110. In turn, the FIR equalizer circuit 110 filters or conditions the signal, in accordance with a predetermined impulse response function, for input to clock data recovery circuit 120.
>
> In general, clock data recovery circuits recover the data at the receiver without receiving the sampling clock from the transmitter (i.e., a separate clock is generated at the receiver). Most clock data recovery circuits "over sample" the data to recover clock and data. In one over sampling method, the incoming data is first sampled at the bit cycle transition point to determine whether the phase of the clock at the receiver leads or lags the phase of the bit transitions in the serial bit stream.

Thon discloses that a sampling clock is generated at the receiver since it is not received from the transmitter. However, this in no way means that the sampling clock generated at the receiver in Thon is unrelated to (independent of) the clock used to recover data. In fact, reference to FIG. 1 of Thon quite clearly shows the dependence of the equalizer (110) and the clock data

recovery circuit (120) on one another as illustrated by the return line going from the top of the clock data recovery circuit block to the top of the equalizer block in FIG. 1.

Further, the Examiner states that in Thon "the clock recovery circuits recover the data at the receiver without the sampling clock from the transmitter . . . ." This is not the same as saying that they are independent of one another, since Thon then explains that the reason that the clock recovery circuits recover the data at the receiver without the sampling clock from the transmitter is because the receiver in Thon generates its own sampling clock.

In contrast, since the claimed equalization technique generates at least one sampling from the received input signal based on a clock signal unrelated to a clock signal used to recover data associated with the received input signal, the claimed equalization technique can operate stand-alone, i.e., without needing input from the CDR circuit for operation.

Thus, the Thon reference fails to supplement the above-noted deficiencies of Ariyavisitakul as applied to claim 1. Accordingly, it is believed that the teachings of Ariyavisitakul and Thon fail to meet the limitations of claim 1.

Also, the Examiner has failed to identify a cogent motivation for combining Ariyavisitakul and Thon in the manner proposed. The Examiner provided the following statement of motivation beginning in the previous Office Action:

> It would have been obvious to one of ordinary skill in the art at the time of invention to use a clock for sampling the received signal unrelated to the clock used for data recovery purposes to make the process of data recovery faster (i.e., without spending time on recovering the clock of the transmitter and by using receiver's local clock).

The present final Office Action at page 3 simply rewords the same assertion. Applicants respectfully submit that these are conclusory statements of the sort rejected by both the Federal Circuit and the U.S. Supreme Court (see KSR v. Teleflex decision cited in previous response). There has been no showing in the present §103(a) rejection of claim 1 of objective evidence of record that would motivate one skilled in the art to combine Ariyavisitakul and Thon to produce the particular limitations in question.

Furthermore, Applicants note that the Office Action mentions using a clock signal is

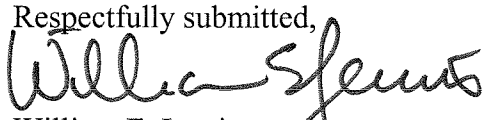
inherent in Ariyavisitakul. However, Applicants still maintain that Ariyavisitakul does not contain the disclosure which is necessary to support a rejection of a claim on the basis of inherency, as set forth in the previous response.

For at least these reasons, Applicants assert that claim 1 is patentable over Ariyavisitakul and Thon. Independent claims 11 and 21 include limitations similar to those of claim 1, and are therefore believed allowable for reasons similar to those described above with reference to claim 1. Dependent claims 3, 9, 10, 13, 19, 20, 22 and 23 are allowable for at least the reasons identified above with regard to claims 1, 11 and 21. One or more of these claims are also believed to define separately-patentable subject matter over the cited art. Accordingly, withdrawal of the §103(a) rejection of claims 1, 3, 9-11, 13 and 19-23 is respectfully requested.

With regard to the §103(a) rejection of claims 2, 4-8, 12 and 14-18, Applicants assert that the Hsu, Dally, Shattil and Best references fail to remedy the deficiencies described above with regard to Ariyavisitakul. Thus, claims 2, 4-8, 12 and 14-18 are patentable at least by virtue of their dependency from claims 1, 11 and 21. Claims 2, 4-8, 12 and 14-18 also recite patentable subject matter in their own right.

In view of the above, Applicants believe that claims 1-23 are in condition for allowance, and respectfully request withdrawal of the §103(a) rejections.

Respectfully submitted,



Date: December 19, 2007

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PRE-APPEAL BRIEF REQUEST FOR REVIEW

Docket Number (Optional)	
YOR920030375US1	

Application Number	Filed
10/668,562	September 23, 2003

First Named Inventor	
Jose A. Tierno	

Art Unit	Examiner
2611	Leila Malek

Applicant requests review of the final rejection in the above-identified application. No amendments are being filed with this request.

This request is being filed with a notice of appeal.

The review is requested for the reason(s) stated on the attached sheet(s).
Note: No more than five (5) pages may be provided.

I am the

- ☐ applicant/inventor.
- ☐ assignee of record of the entire interest.
  See 37 CFR 3.71. Statement under 37 CFR 3.73(b) is enclosed.
  (Form PTO/SB/96)
- ☑ attorney or agent of record. Registration number 39,274.
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Signature

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December 19, 2007
Date

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